



Safeguard Microelectronic Systems from Security Vulnerabilities

Analyz-N[™] Work Flow

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	Input
Security Properties	Chip Design (RTL or Gate-Level)
+	Product
	Output
Trigger Pattern Identification	Security Vulnerabilities Analysis Report
	Design Guidance

Analyz-N[™] & Services



Detects security vulnerabilities in IPs or SoCs at RTL or Gate level to empower IP providers and SoC integrators with broader threat coverage at different levels of abstraction.

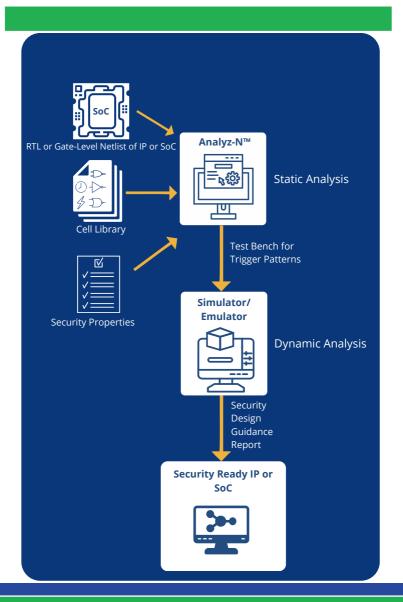
Employs formal methods resulting in high level of confidence and boosts competitive edge.

Offers actionable security report that includes identified assets, security assertions, vulnerable points, stimuli that trigger the vulnerabilties, and mitigation plan.

Offensive Security Assurance Services

- · System and IP Level Threat Modeling
- Automated Asset Identification
- Security Assertion Generation
- Generation of Trigger Patterns
- Vulnerability Analysis
- · Actionable Design Guidance Report to Resolve Vulnerabilities

Commercial Integration



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